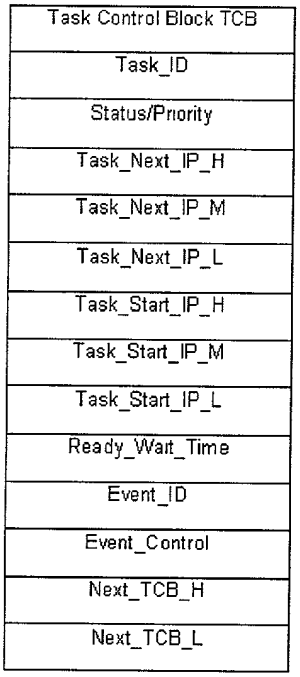

Fig. 1 - Data Memory – Task Control Block

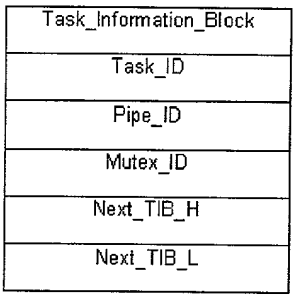

Fig 2 - Data Memory – Task Information Block

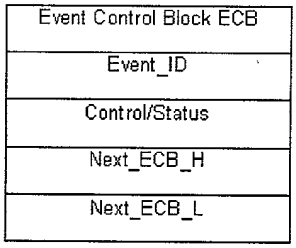

Fig 3 - Data Memory – Event Control Block

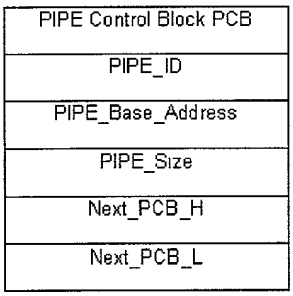

Fig 4 - Data Memory - Pipe Control Block

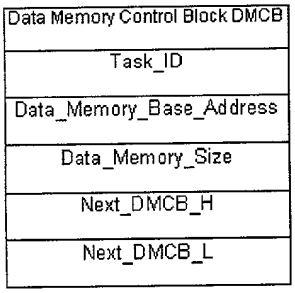

Fig 5 - Data Memory – Data Memory Control Block

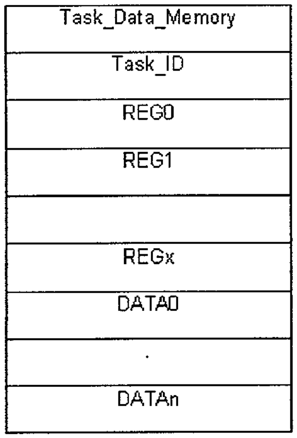

Fig 6 - Data Memory – Task Data Memory

Port_Information_Block
Asignation_Port_Mask_A
Asignation_Port_Mask_B
Asignation_Port_Mask_C
Asignation_Port_Mask_D
Asignation_Port_Mask_E
Asignation_Port_Mask_F
.
Input_Selection_Mask_A
Input_Selection_Mask_B
Input_Selection_Mask_C
Input_Selection_Mask_D
Input_Selection_Mask_E
Input_Selection_Mask_F
Idle_State_Mask_A
Idle_State_Mask_B
Idle_State_Mask_C
Idle_State_Mask_D
Idle_State_Mask_E
Idle_State_Mask_F
.
Idle_State_Mask_A
Idle_State_Mask_B
Idle_State_Mask_C
Idle_State_Mask_D
Idle_State_Mask_E
Idle_State_Mask_F
.
Change_State_A
Change_State_B
Change_State_C
Change_State_D
Change_State_E
Change_State_F
.

Fig.7 - Data Memory – Port Information Block

KERNEL control Registers
DM_Remainder_H
DM_Remainder_L
Max_Priority
Max_Wait_Time
Task_ID_Winner
IP_H
IP_M
IP_M
IP_L
DM_Pointer_H
DM_Pointer_L
TCB_Pointer_H
TCB_Pointer_L
ECB_Pointer_H
ECB_Pointer_L
DMCB_Pointer_H
DMCB_Pointer_L
TIB_Pointer_H
TIB_Pointer_L
PCB_Pointer_H
PCB_Pointer_L
Last_TCB_Pointer_H
Last_TCB_Pointer_L
Last_ECB_Pointer_H
Last_ECB_Pointer_L
Last_TIB_Pointer_H
Last_TIB_Pointer_L
Last_PIB_Pointer_H
Last_PIB_Pointer_L
Last_DMCB_Pointer_H
Last_DMCB_Pointer_L

Fig 8 - Data Memory – Kernel Control Registers

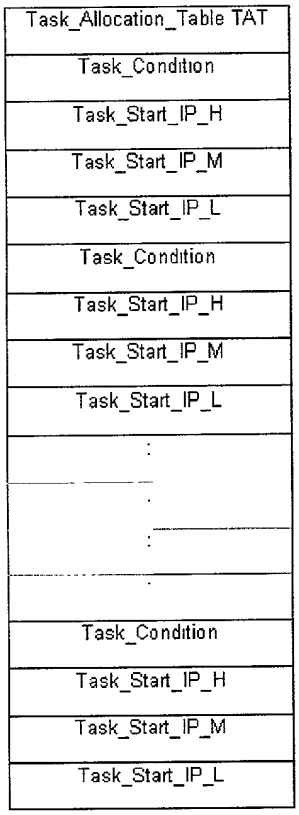

Fig 9 - Program Memory – Task Allocation Table

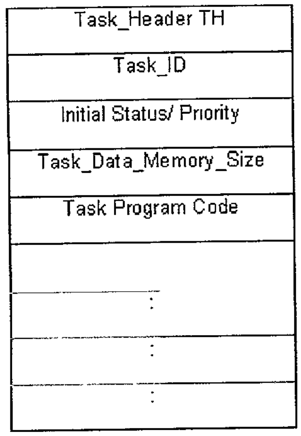

Fig 10 - Program Memory – Task Header

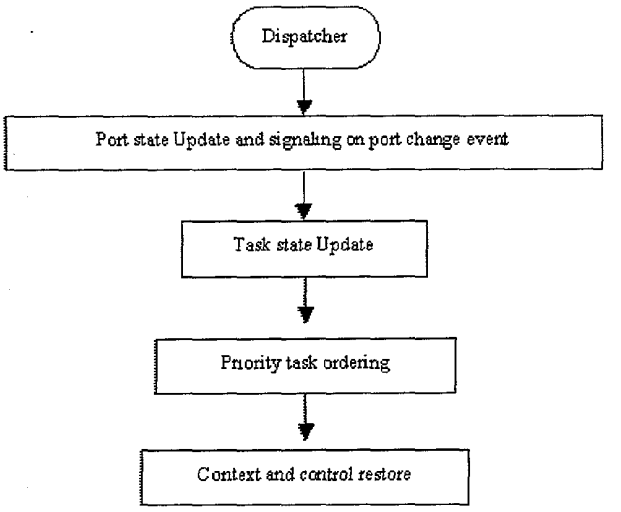

Fig 11 – Kernel – Dispatcher General Flow Chart

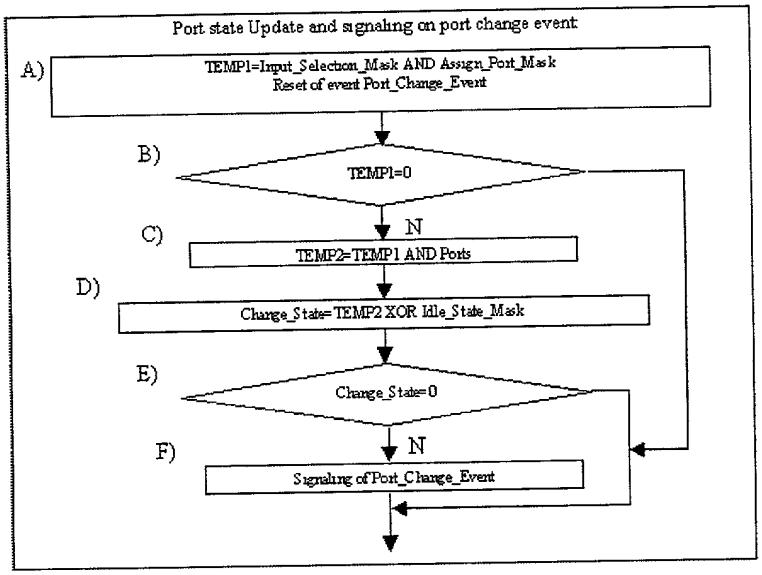

Fig 12 – Kernel – Port State Update

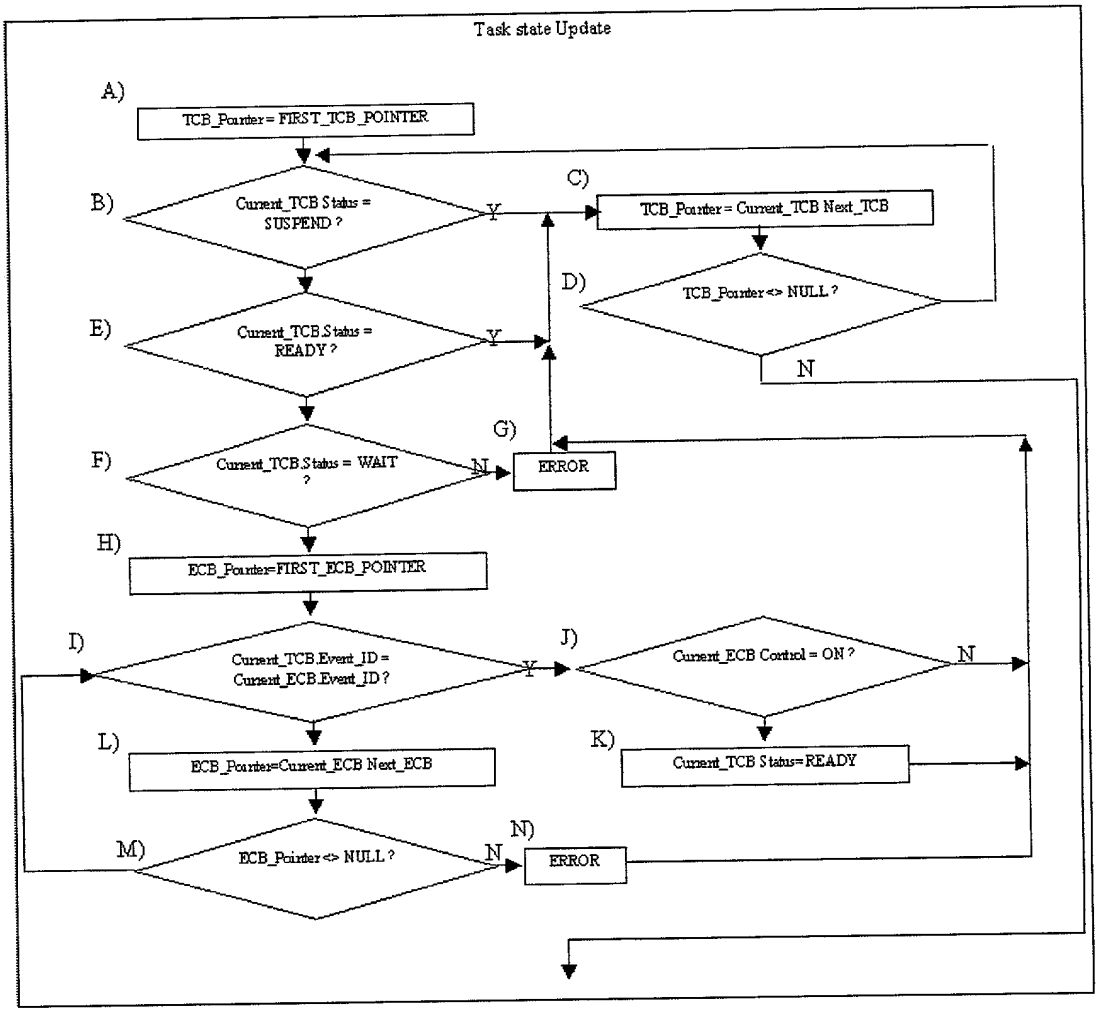

Fig 13 – Kernel – Task State Update

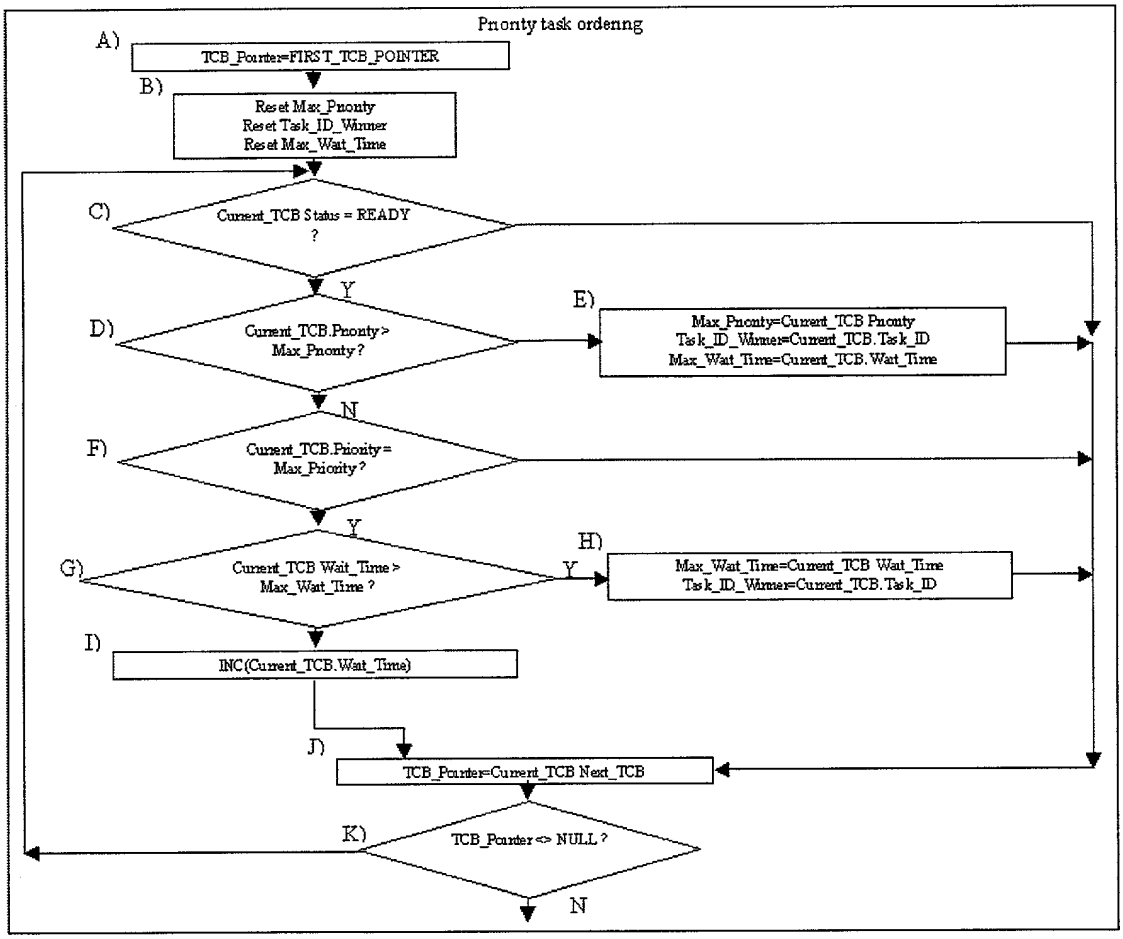

Fig 14 – Kernel – Priority Task Ordering

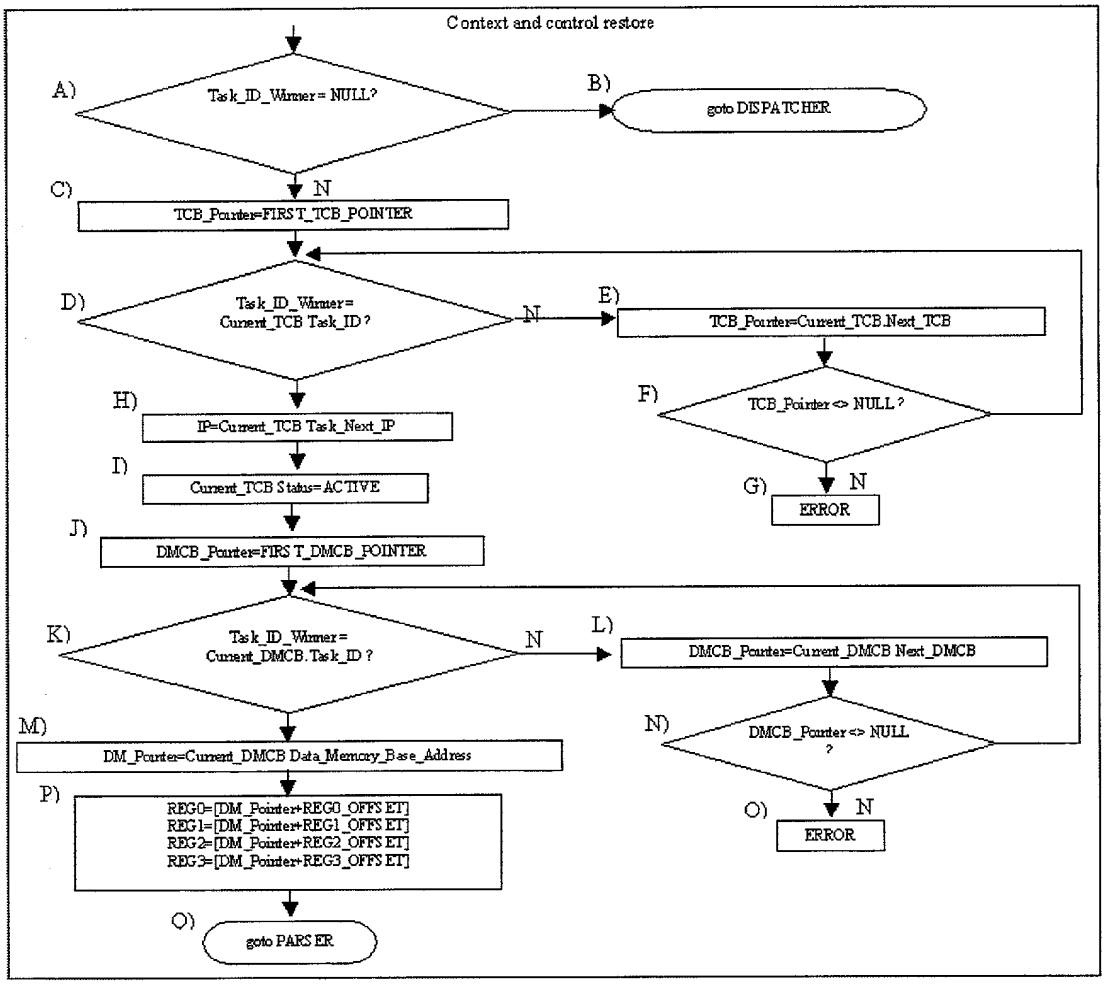

Fig 15 – Kernel – Context and Control Restore